please enter the specification correction on paragraph [0017]. Thank you.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In the specification, page 5, paragraph [0017], line 6, change "R_H" to --R_{HS}--.

2. The following is an examiner's statement of reasons for allowance:

No prior art teaches a current control circuit calibration for an actuator based on the timing and a current value of a high side transistor and a low side transistor.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bentsu Ro whose telephone number is 571 272-2072. The examiner can normally be reached on WS08605.

[0017] In general operation, a gate of the transistor Q_{HS} is discretely enabled and a gate of the transistor Q_{LS} is pulse width modulated (PWM) to provide an average current to the load L_{LOAD}. The load current causes a voltage drop across a sense resistor R_S, which is coupled to one leg of a current mirror circuit 106, which includes, as a component thereof, a high-side resistor R_{HS}, which is coupled between a power supply +V and a terminal (drain) of the transistor Q_{HS}. The processor 102 is programmed to provide a plurality of pulse width modulated (PWM) signals that provide different average set-points, which are voltage signals of different levels, to inputs of a multiplexer (MUX) U5. The processor 102 is also coupled to a plurality of select lines of the MUX U5. The select lines are controlled by the processor 102 (or alternatively control circuit 120) to select one of the set-points provided at the inputs of the MUX U5. An output of the MUX U5 is coupled to a second input of a comparator U3, whose first input is coupled to a high-side of the resistor R_S.

[0018] An output of the comparator U3 is coupled to a first input of the processor 102. The level of the output of the comparator U3 provides an indication to the processor 102 as to whether the current through the resistor R_{HS} is above or below a desired level, set at the second input of the comparator U3 (as provided by the MUX U5). Alternatively, the circuit 120 may be coupled to an output of the comparator U3 to control the select lines of the MUX U5 and, thus, in this embodiment, offload control of the select lines from the processor 102. The voltage at the output of the MUX U5, i.e., at the second input of the comparator U3, corresponds to a desired load current, as determined by the processor 102. The current comparator U3 compares the analog signals provided at its second and first inputs, i.e., provided at the output of the MUX U5 and a voltage dropped across the resistor R_S, thus, providing an indication of whether the high-side load current is at a desired level.

[0019] The processor 102 controls a duty cycle of a control signal provided to a control terminal, i.e., a gate, of the transistor Q_{LS}, via the driver

Correction for
Specification Page 5, para. [0017].